In the Claims:

Please amend claim 13. The claims are as follows:

1. (Withdrawn) A dual damascene structure, comprising:

a first interconnect level comprising a first dielectric layer and including a multiplicity of first damascene or dual damascene conductive wires, each first damascene or dual damascene conductive wire extending from a top surface of said first dielectric layer a distance toward a bottom surface of said first dielectric layer, said distance less than, equal to greater than a thickness of said first dielectric layer;

a second interconnect level directly above and in contact with said first dielectric layer, said second interconnect level comprising a second dielectric layer and including a multiplicity of second dual damascene conductive wires, each second dual damascene conductive wire extending from a top surface of said second dielectric layer a distance toward a bottom surface of said second dielectric layer, said distance less than a thickness of said second dielectric layer; and

a dual damascene conductive via bar within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via bar having a length greater than its width, said length and width of said dual damascene conductive via bar extending in said plane defined by said top surface of said second dielectric layer.

2. (Withdrawn) The structure of claim 1, further including:

a dual damascene conductive via within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via having a length about equal to its width, said length and width of said dual damascene conductive via extending in a plane defined by said top surface of said second dielectric layer.

3. (Withdrawn) The structure of claim 1, further including:

an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires a distance toward said bottom surface of said first dielectric layer, said distance less than a distance between said additional conductive dual damascene via bar and said bottom surface of said first dielectric layer.

4. (Withdrawn) The structure of claim 1, further including:

an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from said top surface of said first dielectric layer a distance toward said bottom surface of said first dielectric layer, said distance less than said thickness of said first dielectric layer.

5. (Withdrawn) The structure of claim 1, wherein said first dielectric layer includes a first dielectric diffusion barrier layer, a bottom surface of said first dielectric diffusion barrier layer being co-extensive with said bottom surface of said first dielectric layer and said second

dielectric layer includes a second dielectric diffusion barrier layer, a bottom surface of said second dielectric diffusion barrier layer being co-extensive with said bottom surface of said second dielectric layer.

6. (Withdrawn) The structure of claim 5, wherein said dielectric diffusion barrier is selected from the group consisting of silicon nitride and silicon carbide.

7. (Withdrawn) The structure of claim 1, further including:

(a) a spiral shaped dual damascene conductive via bar in said first dielectric layer,

(b) a spiral shaped dual damascene conductive via bar in said second dielectric layer; or

(c) spiral shaped dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said spiral shaped dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said spiral shaped dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said spiral shaped dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another.

8. (Withdrawn) The structure of claim 1, further including:

one or more additional interconnect levels, each additional interconnect level including a spiral shaped dual damascene conductive via bar, a top edge of each spiral shaped dual damascene conductive via bars co-planer with a top surface of its corresponding interconnect level and a bottom edge of each spiral shaped dual damascene conductive via bars co-planer with a bottom surface of its corresponding interconnect level, sidewalls of said spiral shaped dual

damascene conductive via bars and sidewalls aligned to one another and stacked in electrical contact on top of one another.

9. (Withdrawn) The structure of claim 1, further including:

(a) a first plate of a capacitor comprising first additional dual damascene conductive via bars and a second plate of said capacitor comprising second additional dual damascene conductive via bars in said second dielectric layer; or

(b) a first plate of a capacitor comprising first additional dual damascene conductive via bars comprising first additional dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said first additional dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said first additional dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said first additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another and a second plate of said capacitor comprising second additional dual damascene conductive via bars comprising second additional dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said second additional dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said second additional dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said second additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another.

10. (Withdrawn) The structure of claim 1, further including:

a first plate of a capacitor comprising first additional dual damascene conductive via bars in additional dielectric layers, sidewalls of said first additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another; and

a second plate of a capacitor comprising second additional dual damascene conductive via bars in said additional dielectric layers, sidewalls of said second additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another;

11. (Withdrawn) The structure of claim 1, wherein said dual damascene conductive wires and said dual damascene conductive via and said dual damascene via bar comprise a same conductor selected from the group consisting of copper, tungsten, aluminum, aluminum-copper alloy, polysilicon, tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof.

12. (Withdrawn) The structure of claim 1, wherein said dielectric layer is selected from the group consisting of silicon oxide, $SiC_xO_yH_z$ and poly(arylene) ether.

13. (Currently Amended) A method of fabricating a dual damascene structure, comprising:

forming a first interconnect level comprising a first dielectric layer and including a multiplicity of first damascene or dual damascene conductive wires, each first damascene or dual damascene conductive wire extending from a top surface of said first dielectric layer a distance

toward a bottom surface of said first dielectric layer, said distance less than a thickness of said first dielectric layer;

forming a second interconnect level directly above and in contact with said first dielectric layer, said second interconnect level comprising a second dielectric layer and including a multiplicity of second dual damascene conductive wires, each second dual damascene conductive wire extending from a top surface of said second dielectric layer a distance toward a bottom surface of said second dielectric layer, said distance less than a thickness of said second dielectric layer; and

forming a dual damascene conductive via bar within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via bar having a length extending in a lengthwise direction greater than [[its]] a width extending in a widthwise direction, said ~~length~~ lengthwise direction and ~~width~~ widthwise direction ~~of said dual damascene conductive via bar extending in~~ perpendicular to each other and parallel to said plane defined by said top surface of said second dielectric layer.

14. (Original) The method of claim 13, further including:

forming a dual damascene conductive via within said second interconnect level and integral with and extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires and a top surface of one of said multiplicity of said first dual damascene conductive wires, said dual damascene conductive via having a length about equal to

its width, said length and width of said dual damascene conductive via extending in a plane defined by said top surface of said second dielectric layer;

15. (Original) The method of claim 13, further including:

forming an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from a bottom surface of one of said multiplicity of said second dual damascene conductive wires a distance toward said bottom surface of said first dielectric layer, said distance less than a distance between said additional conductive dual damascene via bar and said bottom surface of said first dielectric layer.

16. (Original) The method of claim 13, further including:

forming an additional conductive dual damascene via bar within said first interconnect level, said additional conductive via bar extending from said top surface of said first dielectric layer a distance toward said bottom surface of said first dielectric layer, said distance less than said thickness of said first dielectric layer.

17. (Original) The method of claim 13, wherein said first dielectric layer includes a first dielectric diffusion barrier layer, a bottom surface of said first dielectric diffusion barrier layer being co-extensive with said bottom surface of said first dielectric layer and said second dielectric layer includes a second dielectric diffusion barrier layer, a bottom surface of said second dielectric diffusion barrier layer being co-extensive with said bottom surface of said second dielectric layer.

18. (Original) The method of claim 17, wherein said dielectric diffusion barrier is selected from the group consisting of silicon nitride and silicon carbide.

19. (Original) The method of claim 13, further including:

(a) forming a spiral shaped dual damascene conductive via bar in said first dielectric layer,

(b) forming a spiral shaped dual damascene conductive via bar in said second dielectric layer; or

(c) forming spiral shaped dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said spiral shaped dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said spiral shaped dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said spiral shaped dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another.

20. (Original) The method of claim 13, further including:

forming one or more additional interconnect levels, each additional interconnect level including a spiral shaped dual damascene conductive via bar, a top edge of each spiral shaped dual damascene conductive via bars co-planer with a top surface of its corresponding interconnect level and a bottom edge of each spiral shaped dual damascene conductive via bars co-planer with a bottom surface of its corresponding interconnect level, sidewalls of said spiral shaped dual damascene conductive via bars and sidewalls aligned to one another and stacked in electrical contact on top of one another.

21. (Original) The method of claim 13, further including:

(a) forming a first plate of a capacitor comprising first additional dual damascene conductive via bars and a second plate of said capacitor comprising second additional dual damascene conductive via bars in said second dielectric layer; or

(b) forming a first plate of a capacitor comprising first additional dual damascene conductive via bars comprising first additional dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said first additional dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said first additional dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said first additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another and a second plate of said capacitor comprising second additional dual damascene conductive via bars comprising second additional dual damascene conductive via bars in both said first and said second dielectric layers, top edges of said second additional dual damascene conductive via bars co-planer with top surfaces of corresponding dielectric layers and bottoms edged of said second additional dual damascene conductive via bars co-planer with bottom surfaces of said corresponding dielectric layers and sidewalls of said second additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another.

22. (Original) The method of claim 13, further including:

forming a first plate of a capacitor comprising first additional dual damascene conductive via bars in additional dielectric layers, sidewalls of said first additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another; and

forming a second plate of a capacitor comprising second additional dual damascene conductive via bars in said additional dielectric layers, sidewalls of said second additional dual damascene conductive via bars aligned to one another and stacked in electrical contact on top of one another;

23. (Original) The method of claim 13, wherein said dual damascene conductive wires and said dual damascene conductive via and said dual damascene via bar comprise a same conductor selected from the group consisting of copper, tungsten, aluminum, aluminum-copper alloy, polysilicon, tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof.

24. (Previously Presented) The method of claim 13, wherein said dielectric layer is selected from the group consisting of silicon oxide, $SiC_xO_yH_z$ and poly(arylene) ether.

25. (Original) A method of fabricating a dual damascene structure, comprising:

(a) providing a substrate;

(b) forming a dielectric layer on said top surface of said dielectric layer;

(c) forming a via bar opening in said dielectric layer, said via bar opening having a length greater than its width, said length and width of said via bar opening extending in said plane defined by said top surface of and dielectric layer, said via bar opening extending through the entire thickness of said dielectric layer;

(d) etching a first trench in said dielectric layer, said first trench aligned to said via bar opening, said first trench extending from said top surface of said dielectric layer toward a bottom surface of said dielectric layer a distance less than a thickness of said dielectric layer;

(e) applying an anti-reflective coating to a top surface of said dielectric layer, said antireflective coating filling said via bar opening;

(f) applying a masking layer to a top surface of said anti-reflective coating;

(g) etching said antireflective coating from said via bar opening and forming a first trench in said dielectric layer over said via bar opening, said first trench extending from said top surface of said dielectric layer toward said bottom surface of said dielectric layer a distance less than a thickness of said dielectric layer;

(h) removing said masking layer and any remaining antireflective coating; and

(i) filling said first trench and said via bar opening with a conductor.

26. (Original) The method of claim 25,

step (c) further including: forming a via opening, said via opening having a length about equal to its width, said length and width of said visa opening extending in a plane defined by said top surface of and dielectric layer, said via opening extending through the entire thickness of said dielectric layer;

step (d) further including: etching a second trench, and said second trench aligned to said via bar opening, said second trench extending from said top surface of said dielectric layer toward a bottom surface of said dielectric layer a distance less than a thickness of said dielectric layer;

step (e) further including: filling said via opening with said antireflective coating;

step (g) further including: etching said antireflective coating from said via bar opening and forming a second trench in said dielectric layer over said via bar opening, said second trench extending from said top surface of said dielectric layer toward said bottom surface of said dielectric layer a distance less than a thickness of said dielectric layer; and

step (i) further including: filling said second trench and said via bar opening with said conductor.

27. (Original) The method of claim 26, further including:

forming a dielectric diffusion barrier layer between a top surface of said substrate and in contact with a bottom surface of said dielectric layer; and

etching said via opening and said via bar opening through said dielectric diffusion barrier layer in step (g).

28. (Original) The method of claim 27, wherein said dielectric diffusion barrier is selected from the group consisting of silicon nitride and silicon carbide

29. (Original) The method of claim 25, further including:

etching an additional via bar opening in said dielectric layer in step (c);

filling said additional via bar opening with said anti-reflective coating in step (e);

not etching said third trench through said dielectric diffusion barrier layer in step (g); and

filling said additional via bar opening with said conductor in step (i).

30. (Original) The method of claim 25, wherein said conductor is selected from the group consisting of copper, tungsten, aluminum, aluminum-copper alloy, polysilicon, tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride and combinations thereof.

31. (Original) The method of claim 25, wherein said anti-reflective coating has a thickness of between about 400 nm to about 800 nm.

32. (Previously Presented) The method of claim 25, wherein said dielectric material is selected from the group consisting of silicon oxide, $SiC_xO_yH_z$ and poly(arylene) ether.